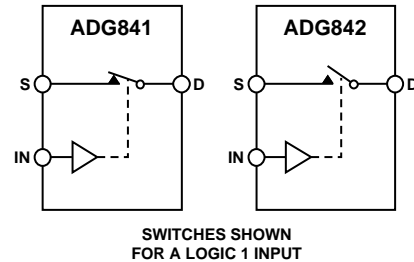


FEATURES
Ultralow on resistance
0.28 Ω typical
0.48 Ω max at 125°C
Excellent audio performance, ultralow distortion
0.025 Ω typical
0.052 Ω max R_{ON} flatness
1.65 V to 3.6 V single supply
High current carrying capability
300 mA continuous current
500 mA peak current
Automotive temperature range: -40°C to +125°C
Rail-to-rail operation
Typical power consumption (<0.01 μ W)
APPLICATIONS
Handsets
PDA's
MP3 players
Power routing
Battery-powered systems
Communication systems
Modems
PCMCIA cards
GENERAL DESCRIPTION

The ADG841 and ADG842 are low voltage CMOS devices containing a single-pole, single-throw (SPST) switch. The ADG841 is closed for a Logic 1 input and the ADG842 is open for a Logic 1 input. The devices offer ultralow on resistance of less than 0.48 Ω over the full temperature range. The ADG841/ADG842 are fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The ADG841/ADG842 exhibit break-before-make switching action.

The ADG841/ADG842 are available in a 6-lead SC70 package.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.
PRODUCT HIGHLIGHTS

1. <0.48 Ω over full temperature range of -40°C to +125°C.
2. Compatible with 1.8 V CMOS logic.
3. High current handling capability (300 mA continuous current at 3.3 V).
4. Low THD + N (0.02% typ).
5. Tiny SC70 package.

Table 1. ADG841/ADG842 Truth Table

| Logic (IN) | ADG841 | ADG842 |
|------------|--------|--------|
| 0 | Off | On |
| 1 | On | Off |

Rev. 0

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REVISION HISTORY

4/05—Revision 0: Initial Version

SPECIFICATIONS—2.7 V TO 3.6 V¹

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|--|-----------|-------------------|--------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | $V_{DD} = 2.7\text{ V}$ |
| On Resistance (R_{ON}) | 0.28 | | | Ω typ | $V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = -100\text{ mA}$ |
| | 0.37 | 0.43 | 0.48 | Ω max | Figure 18 |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.025 | | | Ω typ | $V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = -100\text{ mA}$ |
| | 0.034 | 0.044 | 0.052 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage I_S (OFF) | ± 0.2 | | | nA typ | $V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; Figure 19 |
| Channel On Leakage I_D , I_S (ON) | ± 0.2 | | | nA typ | $V_S = V_D = 0.6\text{ V or }3.3\text{ V}$; Figure 20 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3.2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t_{ON} | 10.5 | | | ns typ | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ |
| | 14 | 15.5 | 16.5 | ns max | $V_S = 1.5\text{ V}$; Figure 21 |
| t_{OFF} | 6.5 | | | ns typ | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ |
| | 7.8 | 8 | 8.2 | ns max | $V_S = 1.5\text{ V}$; Figure 21 |
| Charge Injection | 200 | | | pC typ | $V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Figure 22 |
| Off Isolation | −54 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Figure 23 |
| Total Harmonic Distortion (THD + N) | 0.012 | | | % | $R_L = 32\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 3\text{ V p-p}$ |
| Insertion Loss | −0.02 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Figure 24 |
| −3 dB Bandwidth | 21 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Figure 24 |
| C_S (OFF) | 160 | | | pF typ | |
| C_D (OFF) | 160 | | | pF typ | |
| C_D , C_S (ON) | 238 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.003 | | | μA typ | $V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V |
| | | 1 | 4 | μA max | |

¹ Temperature range is -40°C to $+125^\circ\text{C}$

² Guaranteed by design; not subject to production test.

ADG841/ADG842

SPECIFICATIONS—2.5 V ± 0.2 V¹

V_{DD} = 2.5 V ± 0.2 V, GND = 0 V, unless otherwise noted.

Table 3.

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|-------|-------------------|------------------------|---------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V _{DD} | V | |
| On Resistance (R _{ON}) | 0.3 | | | Ω typ | V _{DD} = 2.3 V, V _S = 0 V to V _{DD} , I _{DS} = −100 mA |
| | 0.35 | 0.4 | 0.45 | Ω max | Figure 18 |
| On Resistance Flatness (R _{FLAT(ON)}) | 0.025 | | | Ω typ | V _{DD} = 2.3 V, V _S = 0 V to V _{DD} , I _{DS} = −100 mA |
| | 0.04 | 0.05 | 0.05 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage I _S (OFF) | ±0.2 | | | nA typ | V _{DD} = 2.7 V |
| Channel On Leakage I _D , I _S (ON) | ±0.2 | | | nA typ | V _S = 0.6 V/2.4 V, V _D = 2.4 V/0.6 V; Figure 19 |
| | | | | | V _S = V _D = 0.6 V or 2.4 V; Figure 20 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V _{INH} | | | 1.7 | V min | |
| Input Low Voltage, V _{INL} | | | 0.7 | V max | |
| Input Current, I _{INL} or I _{INH} | 0.005 | | | μA typ | V _{IN} = V _{INL} or V _{INH} |
| | | | ±0.1 | μA max | |
| Digital Input Capacitance, C _{IN} | 3.2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t _{ON} | 13 | | | ns typ | R _L = 50 Ω, C _L = 35 pF |
| | 16.5 | 18 | 19 | ns max | V _S = 1.5 V; Figure 21 |
| t _{OFF} | 7 | | | ns typ | R _L = 50 Ω, C _L = 35 pF |
| | 8.2 | 8.4 | 8.6 | ns max | V _S = 1.5 V; Figure 21 |
| Charge Injection | 150 | | | pC typ | V _S = 1.25 V, R _S = 0 Ω, C _L = 1 nF; Figure 22 |
| Off Isolation | −54 | | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; Figure 23 |
| Total Harmonic Distortion (THD + N) | 0.022 | | | % | R _L = 32 Ω, f = 20 Hz to 20 kHz, V _S = 1.5 V p-p |
| Insertion Loss | −0.02 | | | dB typ | R _L = 50 Ω, C _L = 5 pF; Figure 24 |
| −3 dB Bandwidth | 21 | | | MHz typ | R _L = 50 Ω, C _L = 5 pF; Figure 24 |
| C _S (OFF) | 170 | | | pF typ | |
| C _D (OFF) | 170 | | | pF typ | |
| C _D , C _S (ON) | 238 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| I _{DD} | 0.003 | | | μA typ | V _{DD} = 2.7 V |
| | | 1 | 4 | μA max | Digital inputs = 0 V or 2.7 V |

¹ Temperature range is −40°C to +125°C.

² Guaranteed by design; not subject to production test.

SPECIFICATIONS—1.65 V TO 1.95¹

V_{DD} = 1.65 V to 1.95 V, GND = 0 V, unless otherwise noted.

Table 4.

| Parameter | +25°C | –40°C to +85°C | –40°C to +125°C | Unit | Test Conditions/Comments |
|--|-----------|-------------------|--------------------|--------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 0.37 | | | Ω typ | $V_{DD} = 1.8$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = -100$ mA |
| | 0.4 | 0.84 | 0.84 | Ω max | Figure 18 |
| | 0.6 | 1.8 | 1.8 | Ω max | $V_{DD} = 1.65$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = -100$ mA |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.17 | | | Ω typ | $V_{DD} = 1.65$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = -100$ mA |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage I_S (OFF) | ± 0.2 | | | nA typ | $V_{DD} = 1.95$ V |
| Channel On Leakage I_D, I_S (ON) | ± 0.2 | | | nA typ | $V_S = 0.6$ V/1.65 V, $V_D = 1.65$ V/0.6 V; Figure 19 |
| | | | | | $V_S = V_D = 0.6$ V or 1.65 V; Figure 20 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | $0.65 V_{DD}$ | V min | |
| Input Low Voltage, V_{INL} | | | $0.35 V_{DD}$ | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μ A typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μ A max | |
| Digital Input Capacitance, C_{IN} | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t_{ON} | 19 | | | ns typ | $R_L = 50 \Omega$, $C_L = 35$ pF |
| | 26 | 28 | 30 | ns max | $V_S = 1.5$ V; Figure 21 |
| t_{OFF} | 8 | | | ns typ | $R_L = 50 \Omega$, $C_L = 35$ pF |
| | 9.5 | 9.8 | 10 | ns max | $V_S = 1.5$ V; Figure 21 |
| Charge Injection | 100 | | | pC typ | $V_S = 1$ V, $R_S = 0$ V, $C_L = 1$ nF; Figure 22 |
| Off Isolation | –54 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; Figure 23 |
| Total Harmonic Distortion (THD + N) | 0.14 | | | % | $R_L = 32 \Omega$, $f = 20$ Hz to 20 kHz, $V_S = 1.2$ V p-p |
| Insertion Loss | –0.02 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5$ pF; Figure 24 |
| –3 dB Bandwidth | 21 | | | MHz typ | $R_L = 50 \Omega$, $C_L = 5$ pF; Figure 24 |
| C_S (OFF) | 178 | | | pF typ | |
| C_D (OFF) | 178 | | | pF typ | |
| C_D, C_S (ON) | 238 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.003 | | | μ A typ | $V_{DD} = 1.95$ V |
| | | 1 | 4 | μ A max | Digital inputs = 0 V or 1.95 V |

¹ Temperature range –40°C to +125°C.

² Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

| Parameter | Rating |
|-----------------------------------|--|
| V _{DD} to GND | −0.3 V to +4.6 V |
| Analog Inputs ¹ | −0.3 V to V _{DD} + 0.3 V |
| Digital Inputs ¹ | −0.3 V to 4.6 V or 10 mA, whichever occurs first |
| Peak Current, S or D | |
| 3.3 V Operation | 500 mA |
| 2.5 V Operation | 460 mA |
| 1.8 V Operation | 420 mA (pulsed at 1 ms, 10% duty cycle max) |
| Continuous Current, S or D | |
| 3.3 V Operation | 300 mA |
| 2.5 V Operation | 275 mA |
| 1.8 V Operation | 250 mA |
| Operating Temperature Range | |
| Automotive (Y Version) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| SC70 Package | |
| θ _{JA} Thermal Impedance | 494.8°C/W |
| Reflow Soldering (Pb-free) | |
| Peak Temperature | 260(+0/−5)°C |
| Time at Peak Temperature | 10 sec to 40 sec |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

¹ Overvoltages at S or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

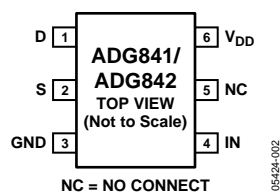


Figure 2. 6-Lead SC70

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|---|
| 1 | D | Drain Terminal. Can be an input or output. |
| 2 | S | Source Terminal. Can be an input or output. |
| 3 | GND | Ground (0 V) Reference. |
| 4 | IN | Logic Control Input. |
| 5 | NC | No Connect. |
| 6 | V _{DD} | Most Positive Power Supply Potential. |

TYPICAL PERFORMANCE CHARACTERISTICS

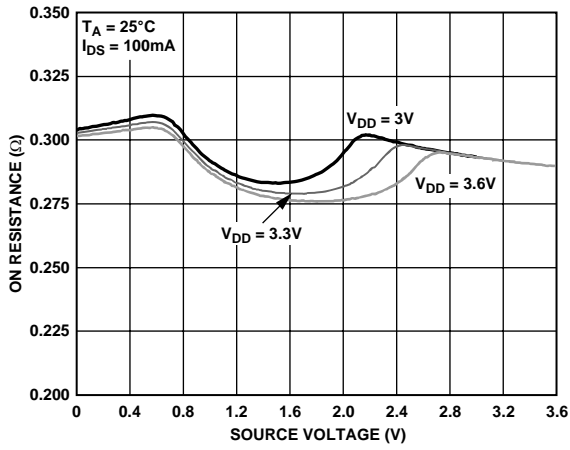


Figure 3. On Resistance vs. V_D (Vs) $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$

05424-003

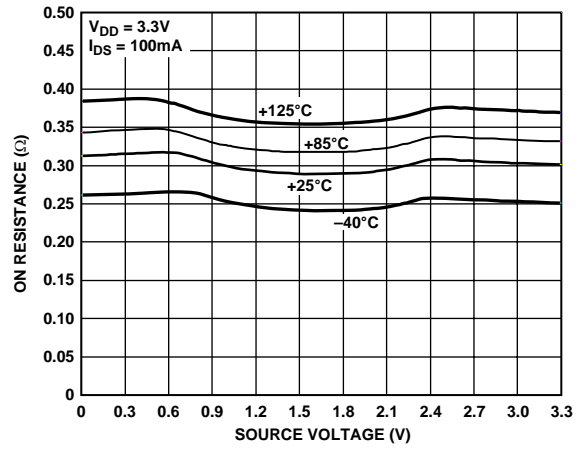


Figure 6. On Resistance vs. V_D (Vs) for Different Temperatures, $V_{DD} = 3.3\text{ V}$

05424-006

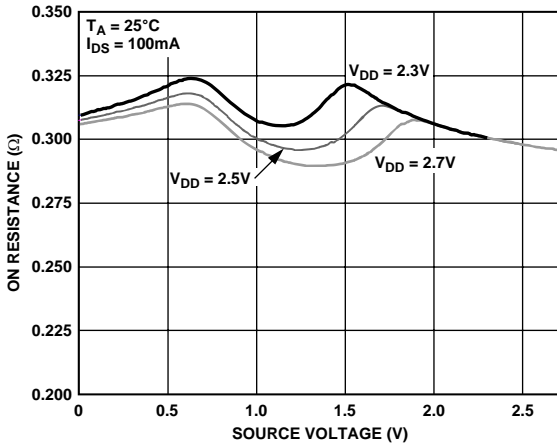


Figure 4. On Resistance vs. V_D (Vs) $V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$

05424-004

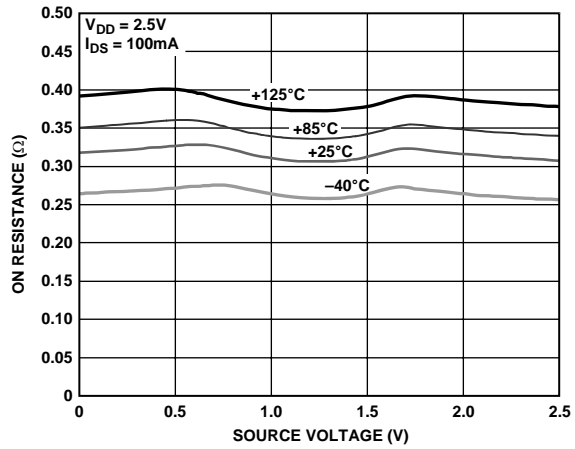


Figure 7. On Resistance vs. V_D (Vs) for Different Temperatures, $V_{DD} = 2.5\text{ V}$

05424-007

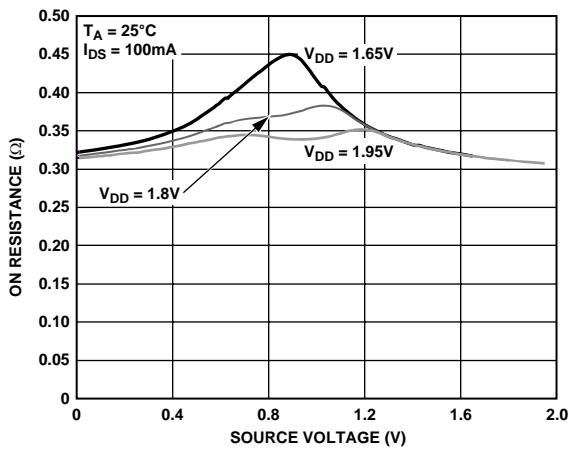


Figure 5. On Resistance vs. V_D (Vs) $V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$

05424-005

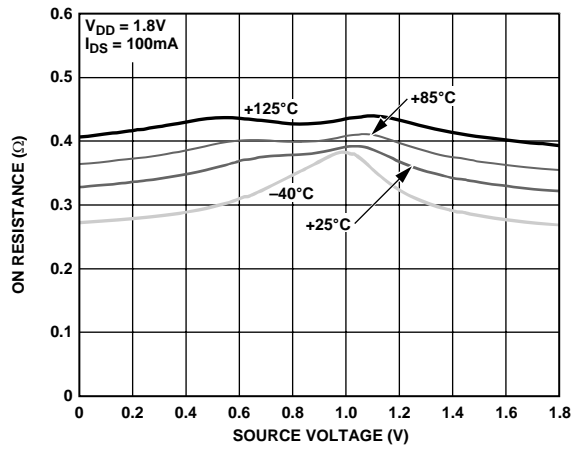


Figure 8. On Resistance vs. V_D (Vs) for Different Temperatures, $V_{DD} = 1.8\text{ V}$

05424-008

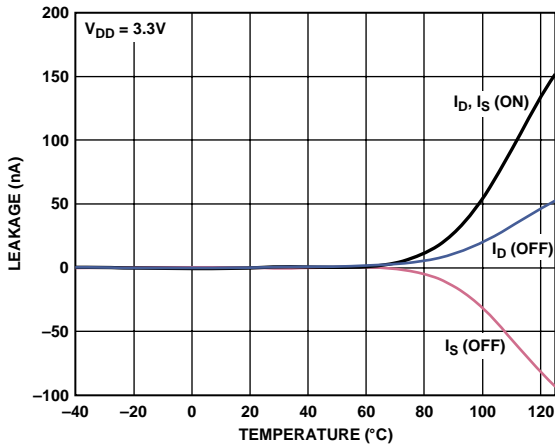


Figure 9. Leakage Current vs. Temperature, $V_{DD} = 3.3V$

05424-009

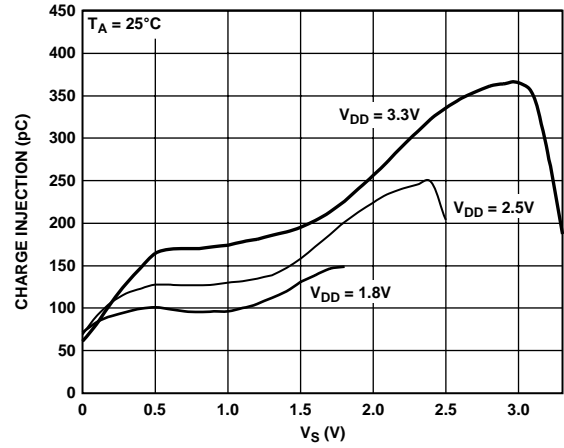


Figure 12. Charge Injection vs. Source Voltage

05424-012

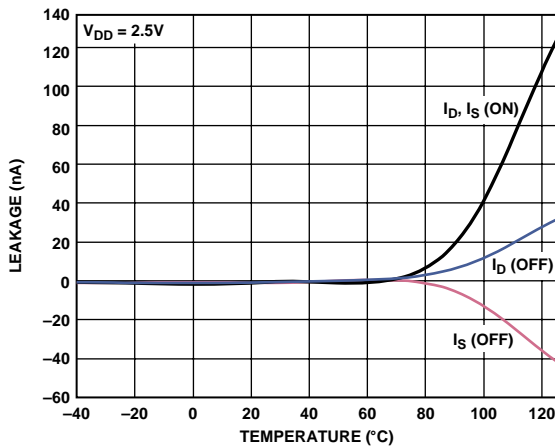


Figure 10. Leakage Current vs. Temperature, $V_{DD} = 2.5V$

05424-010

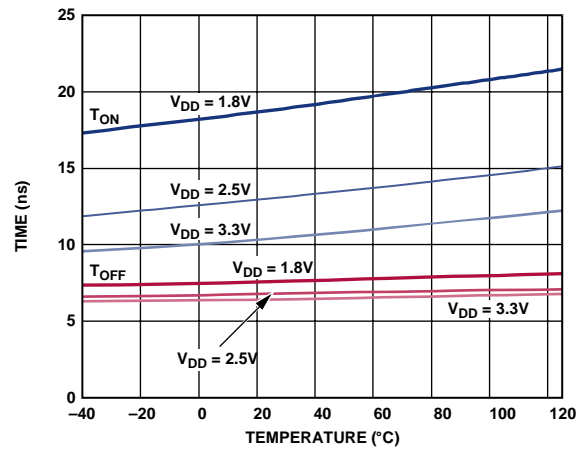


Figure 13. t_{ON}/t_{OFF} Times vs. Temperature

05424-013

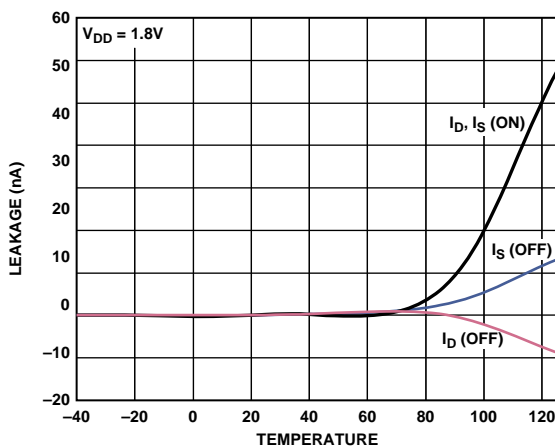


Figure 11. Leakage Current vs. Temperature, $V_{DD} = 1.8V$

05424-011

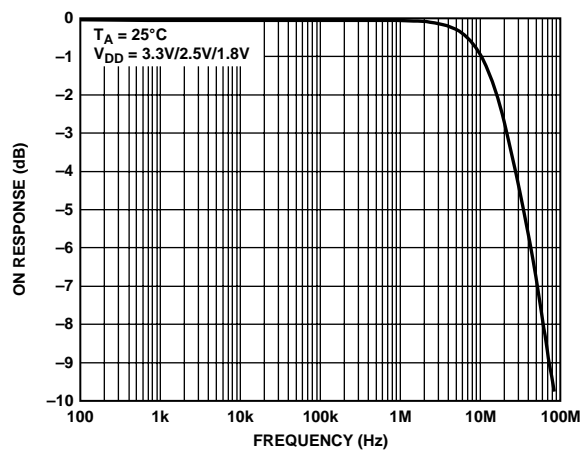


Figure 14. Bandwidth

05424-014

ADG841/ADG842

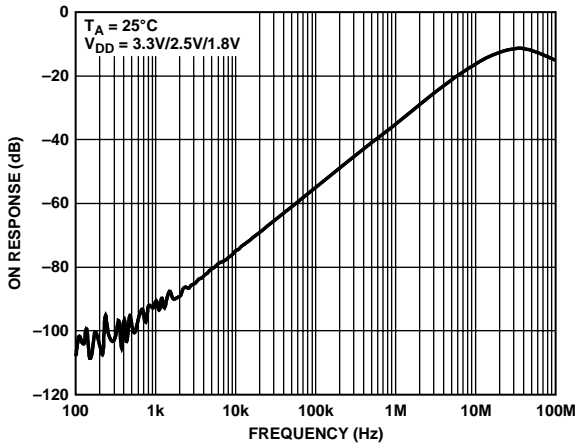


Figure 15. Off Isolation vs. Frequency

05-024-015

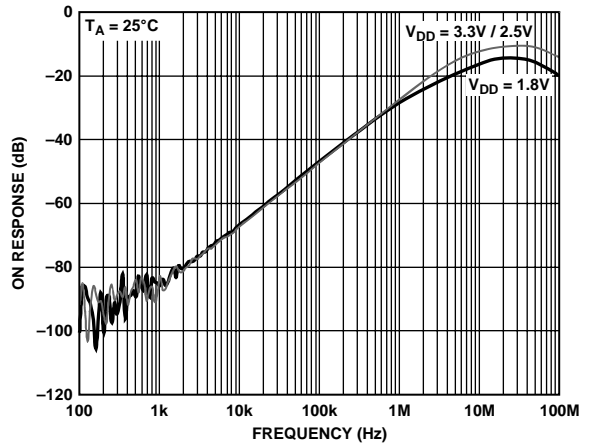


Figure 17. AC PSRR

05-024-017

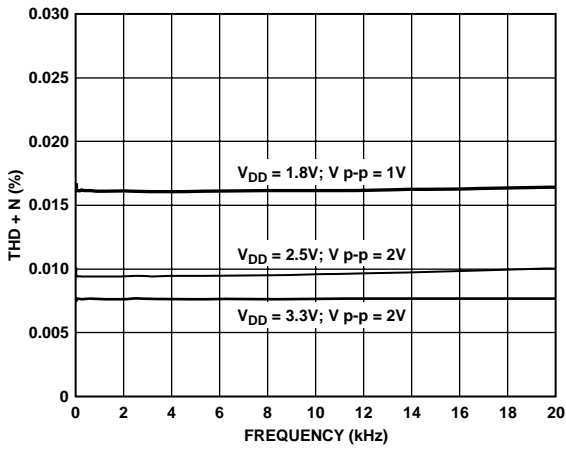


Figure 16. Total Harmonic Distortion + Noise

05-024-016

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on Terminals D and S.

R_{ON}

Ohmic resistance between D and S.

R_{FLAT} (ON)

Flatness is the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (OFF)

Source leakage current with the switch off.

I_D (OFF)

Drain leakage current with the switch off.

I_D, I_S (ON)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (OFF)

Off switch source capacitance. Measured with reference to ground.

C_D (OFF)

Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (ON)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 90% points of the digital input and switch off condition.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

-3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonics amplitude plus noise of a signal to the fundamental.

PSRR

Power Supply Rejection Ratio. This is a measure of the coupling of unwanted ac signals on the power supply to the switch output when the supply is not decoupled.

TEST CIRCUITS

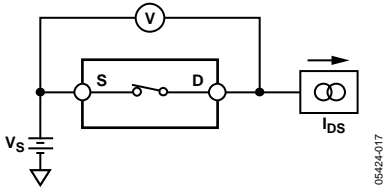


Figure 18. On Resistance

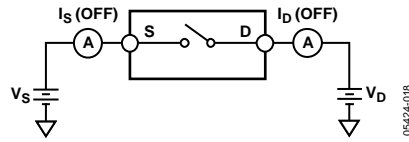


Figure 19. Off Leakage

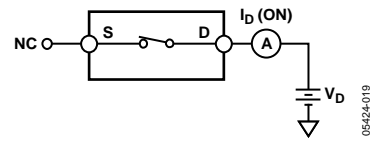


Figure 20. On Leakage

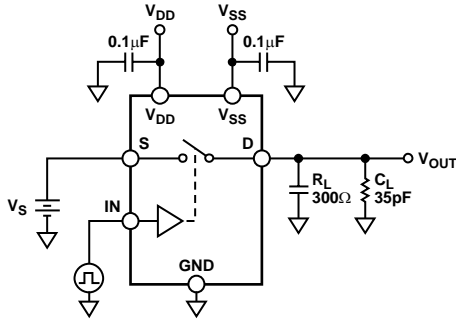


Figure 21. Switching Times, t_{ON} , t_{OFF}

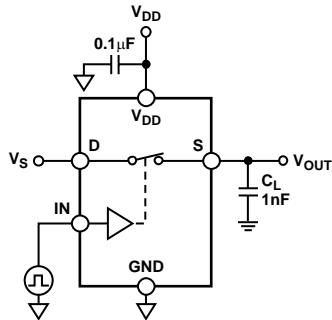
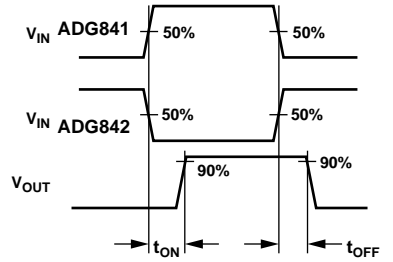
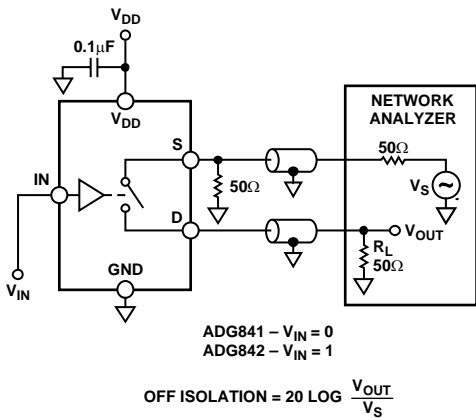
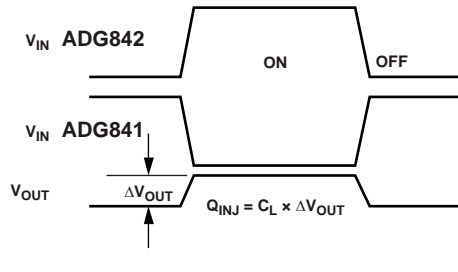


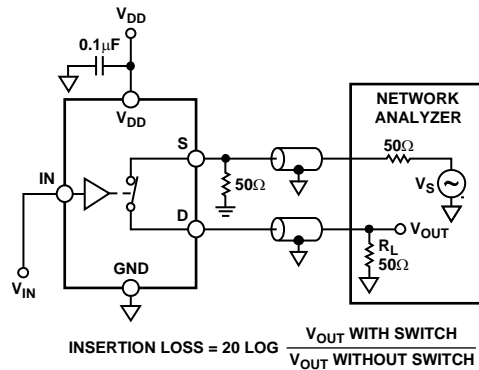
Figure 22. Charge Injection



ADG841 - $V_{IN} = 0$
 ADG842 - $V_{IN} = 1$

$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{OUT}}{V_S}$$

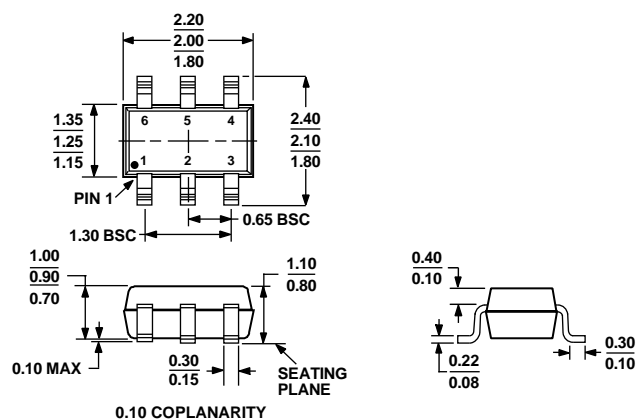
Figure 23. Off Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

Figure 24. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 25. 6-Lead Thin Shrink Small Outline Transistor [SC70]
(KS-6)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding ¹ |
|--------------------------------|-------------------|--|----------------|-----------------------|
| ADG841YKSZ-500RL7 ² | -40°C to +125°C | 6-Lead Thin Shrink Small Outline Transistor (SC70) | KS-6 | SVA |
| ADG841YKSZ-REEL ² | -40°C to +125°C | 6-Lead Thin Shrink Small Outline Transistor (SC70) | KS-6 | SVA |
| ADG841YKSZ-REEL7 ² | -40°C to +125°C | 6-Lead Thin Shrink Small Outline Transistor (SC70) | KS-6 | SVA |
| ADG842YKSZ-500RL7 ² | -40°C to +125°C | 6-Lead Thin Shrink Small Outline Transistor (SC70) | KS-6 | SWA |
| ADG842YKSZ-REEL ² | -40°C to +125°C | 6-Lead Thin Shrink Small Outline Transistor (SC70) | KS-6 | SWA |
| ADG842YKSZ-REEL7 ² | -40°C to +125°C | 6-Lead Thin Shrink Small Outline Transistor (SC70) | KS-6 | SWA |

¹ Branding on this package is limited to three characters due to space constraints.

² Z = Pb-free part.

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